Power Conscious BIST Approaches

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Today’s VLSI circuits and systems

- Test costs become significant
  - Built-In Self-Test

- Power consumption
  - High activity during the test phase

➔ Low power BIST approaches
1. Introduction

2. Power consumption

3. Power consideration during BIST

4. Functional BIST

5. Conclusion & Perspectives
1. Introduction - Context

- Built-In Self Test Principle
  - Test pattern generator
  - and signature analyzer inserted in the design

- Advantages
  - Low cost external test equipment
  - Test performed at the maximum system speed
  - Lower test time by concurrent testing
  - High defect coverage due to a large amount of patterns
  - Test in situ
  - Protecting intellectual property (System-on-Chip)
1. Introduction - BIST Approaches

- Test per-scan
  - Scan design
  - Serial test resources

Diagram:
- Circuit Under Test
  - Scan Chain
    - Test Pattern Generator
    - Test Controller
    - Signature Analyzer
  - Low Cost External Tester
1. Introduction - BIST Approaches

- Test per-clock
  - Parallel test
  - At-speed
1. Introduction - Problematic and Purpose

- During the BIST: Test phase
  - Test efficiency is correlated with the toggle rate
  - DfT like SCAN are intensively used in test mode
    - High activity during the test phase
    - High power consumption

- Purpose
  - Decrease the power consumption
    - Standard BIST techniques
      - like test per-scan and test per-clock
    - New approach: Functional BIST
2. Power Consumption

- Power consumption in a CMOS design
  - Dynamic power is the dominant source of power
- Power parameters
  - Energy
    - Battery lifetime for portable equipment
  - Average Power
    - Hot spots
    - Bonding wires
    - Package damage
  - Peak Power
    - Burn-out
    - Bad function
    - Destruction
3. Low Power BIST - State of the Art

- Decrease the power consumption during the test

  ➢ Industrial solutions: ad-hoc
    - Oversizing power supply, package and cooling
    - Breaks in the test process
    - Test with reduced operation frequency

  ➢ Academic research
    - Distributed BIST control scheme
    - Circuit partitioning
    - Low power DfT
    - Vector filtering architectures
    - Low power test pattern generator
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Basic view of a sequential circuit
3. Low Power BIST - Low Power DfT

- Scan flip-flop: Multiplexor

![Diagram showing combinational logic and scan flip-flops]
- Scan chain

```
Combinational Logic
```

```
Scan In  Q  Q  Scan Out
D   D   D
sdi  sdi  sdi
Test Enable
```
Modified scan chain

Combinational Logic

Scan In → D → Q
Test Enable

Scan Out → D → Q

What are the necessary test patterns?

Pseudo-random test sequence
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- Pseudo-random test sequence
- Desired fault coverage
- Patterns detect new faults
3. Low Power BIST - Vector Filtering Architecture

What are the necessary test patterns?

- Pseudo-random test sequence
  - Patterns detect new faults
  - Patterns don’t detect new faults

Desired fault coverage

Implementation

- Pattern counter and clock tree modification
3. Low Power BIST - Results

- When the both techniques are used
  - In the circuit
    - Lower power DfT
  - In the scan chain and in the clock tree
    - Vector filtering architecture

- Power consumption
  - Approximately 2 % of the original power are required

- Area overhead
  - Less than 10 % for large designs
Standard pseudo-random BIST approach

- Each circuit input can change at each clock cycle
  - High switching activity
  - and high power consumption
3. Low Power BIST - Test per-clock

- Low activity generator

- Only half of the circuit input can change at each clock cycle
  - Power consumption reduction is between 48% and 94%
  - Negligible cost in terms of area overhead

4. Functional BIST - Purpose

- Test problems linked to processor design
  - Standard BIST approaches
    - Pseudo-random pattern resistance
    - Area overhead
    - Performance degradation
    - Power consumption

- Generate tests with the help of the functionality
  - Functional BIST approach
    - Structural faults
    - No additional dedicated hardware
Processor application

- Test resources (TPG and SA) obtained by programming
- External tester
  - Configuration downloading
  - Response analysis
4. Functional BIST - Power Consumption

- **Design used**
  - The LEON processor
  - *Open sources*

- **Standard BIST scheme**
  - Additional test mode
  - Test data / Functional data

- **Functional BIST**
  - Tests applied in the standard operation mode
  - Functional instructions are used

⇒ Functional BIST approach should keep power consumption values in the range of the system’s specification
5. Conclusion

- Problems of recent VLSI circuits and systems
  - Test cost
    - BIST approaches
  - Power consumption in the test phase
    - High activity due to non-functional test data

- Low power BIST techniques
  - Test per-scan
    - Reduction by 98% obtained
  - Test per-clock
    - Reduction by 48% to 94% obtained
  - On going work
    - Functional BIST
5. Perspectives

- Implement a functional BIST approach for the LEON processor
  - Structural faults
    - Stuck-at faults, ...
  - Tests generation
    - Tests instructions ⇒ Instructions set
    - Tests data ⇒ Power constraints

- Power consumption comparisons
  - Functional BIST / Standard BIST techniques