
Efficient Architectures for Signal Detection in MIMO Systems

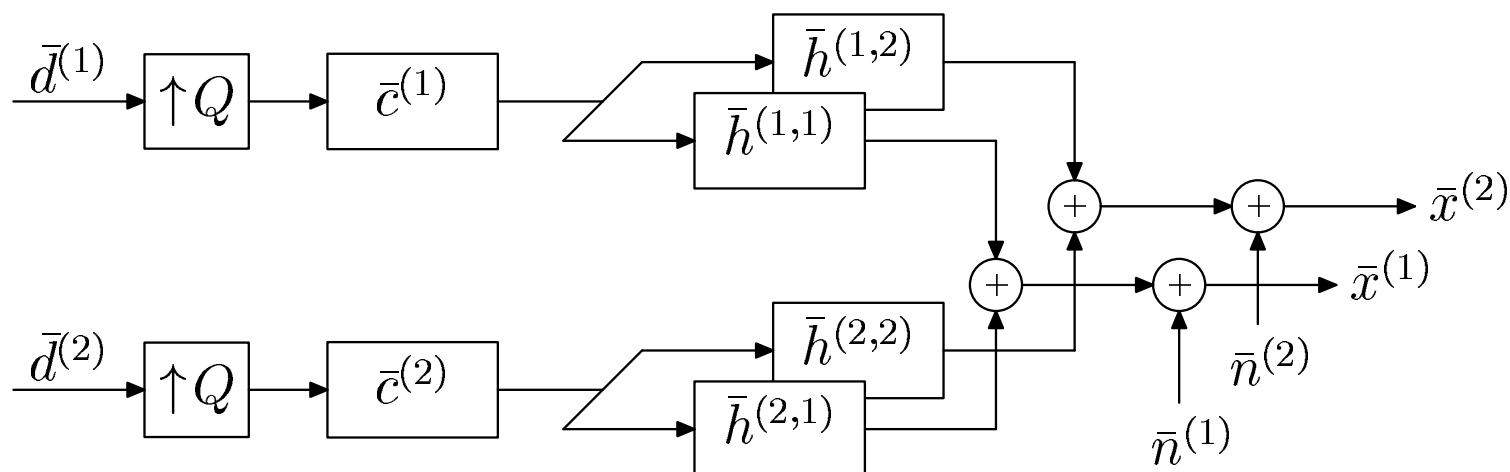
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System can be characterized with a *block* impulse response; elements are matrices. Convolution as system of linear equations:

$$\mathbf{x} = \mathbf{T}\mathbf{d} + \mathbf{n}$$

Signal (or Data) Detection via Linear Estimation (*Least Squares, Gauss-Markov, ...*).

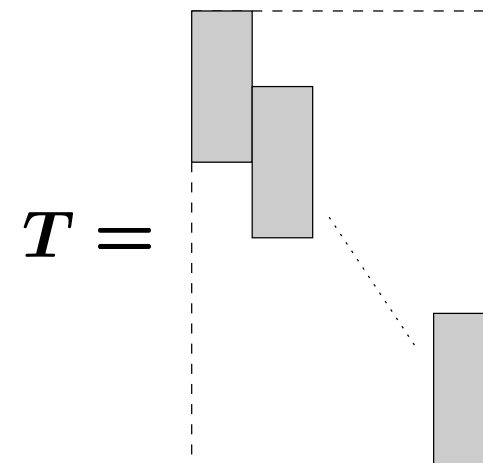
$$\hat{\mathbf{d}} = (\mathbf{T}^H\mathbf{T})^{-1}\mathbf{T}^H\mathbf{x}$$

System ist time invariant and has limited ISI

→ T is Block-Toeplitz and band structured.

Significant noise level and thresholding

→ Approximate estimates might be good enough



Computation of \hat{d} with *Displacement Representation* and *Schur Algorithm* (based on local transformations)

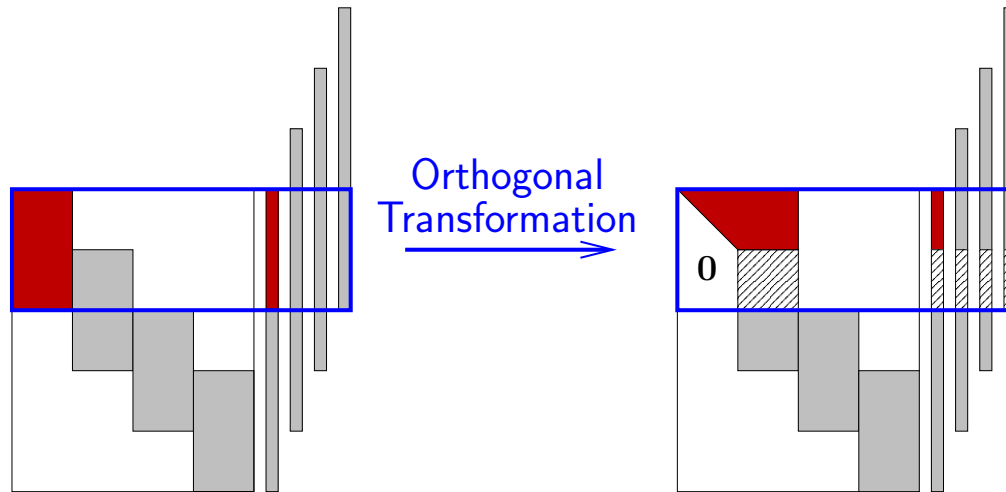
Implementation on a parallel processor array

Implementation of the local transformations via CORDIC

Schur Algorithm with Displacement Representation

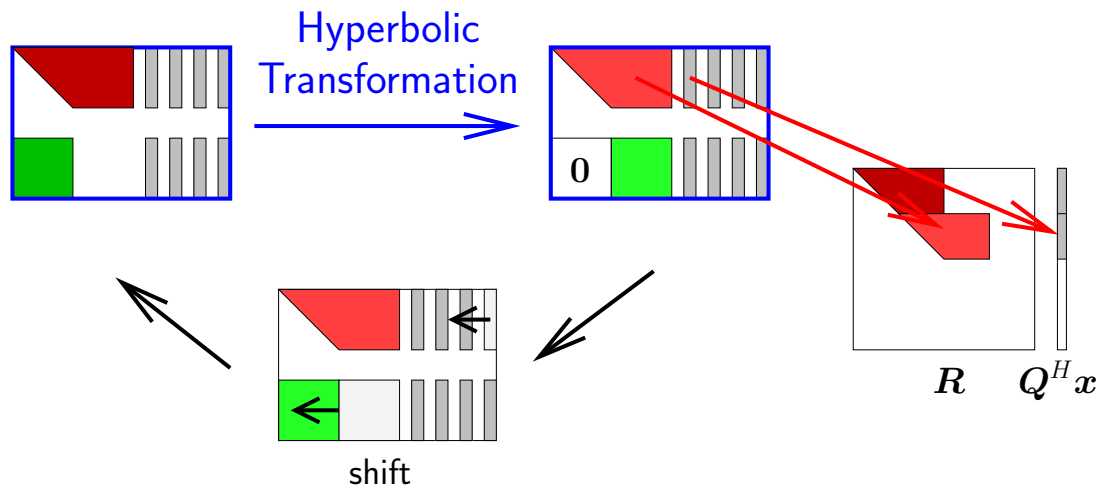
Displacement Representation consists of *generators*.
Computation via partial QR decomposition.

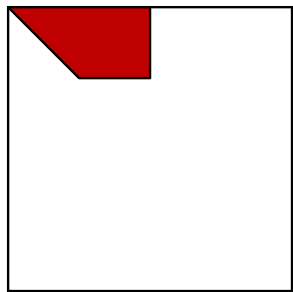
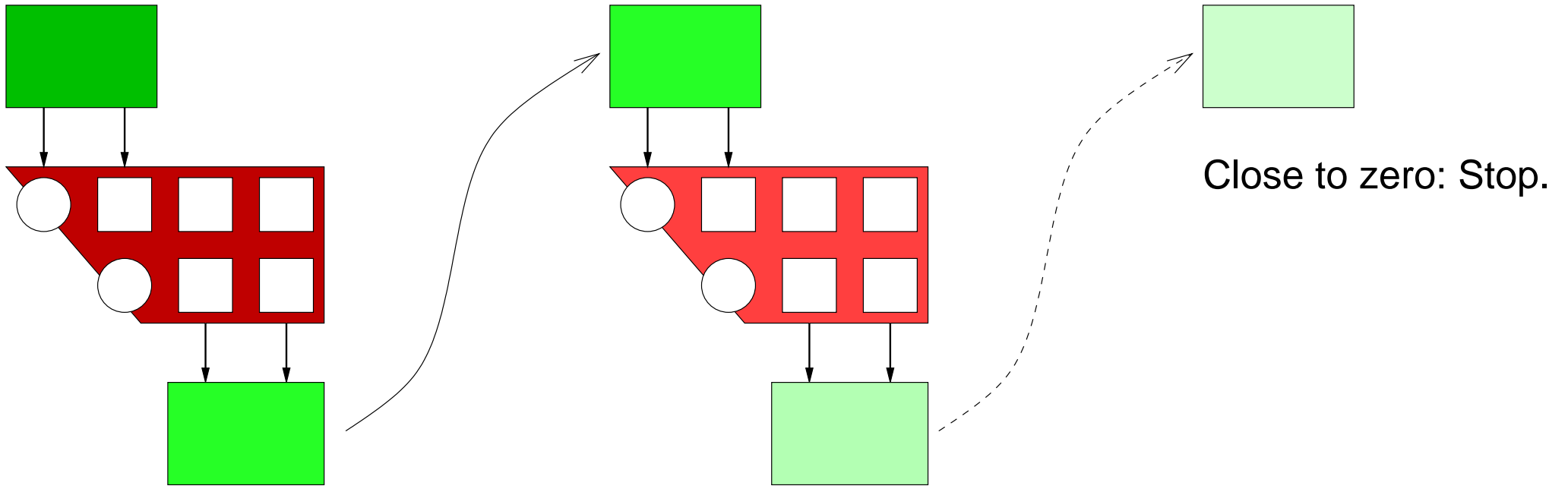
processor array with orthogonal cells



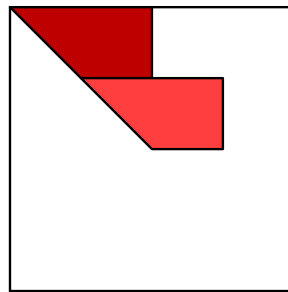
Completion of QR decomposition via repeated Schur steps.

processor array with hyperbolic cells

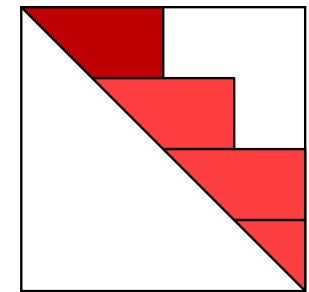




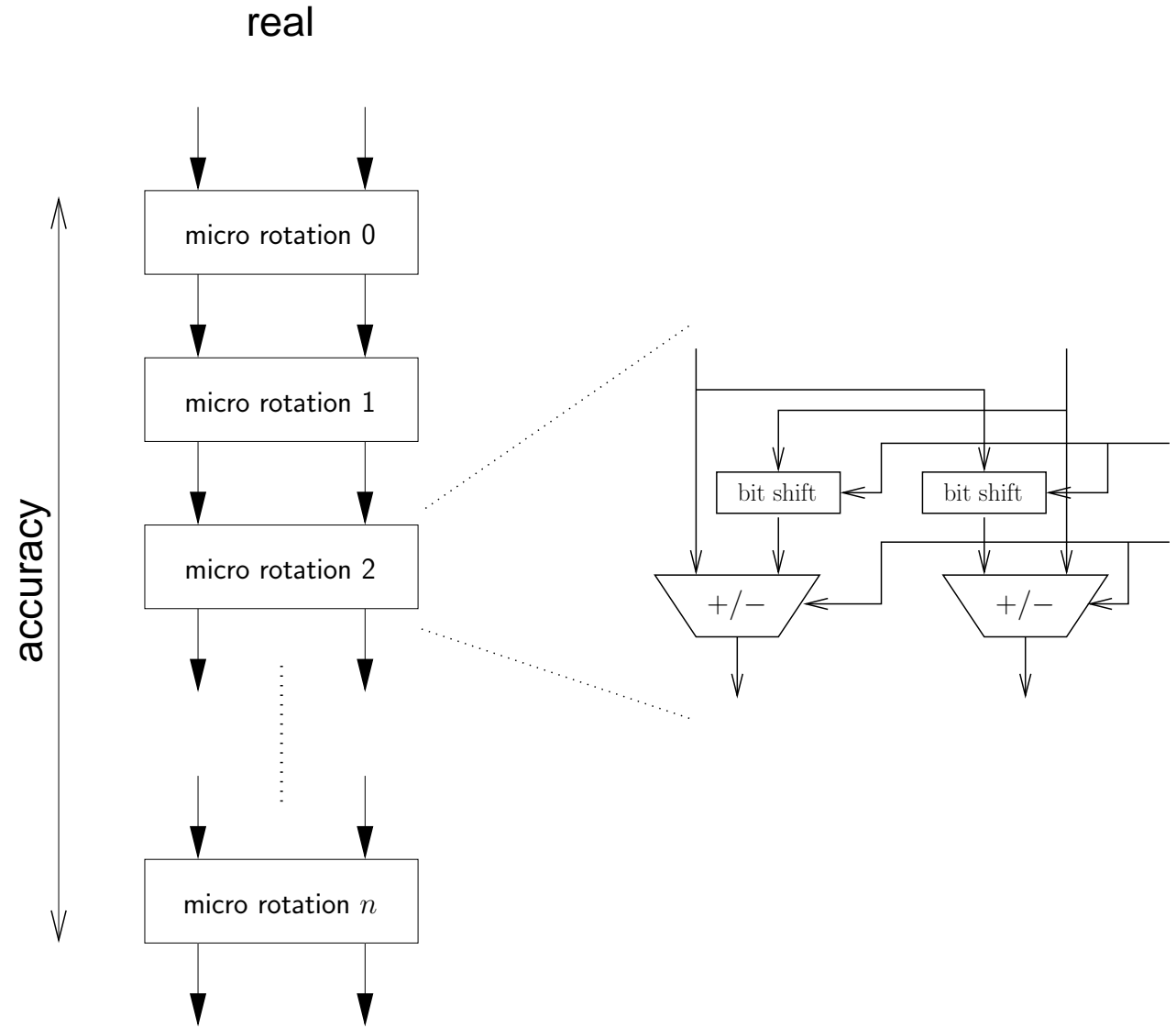
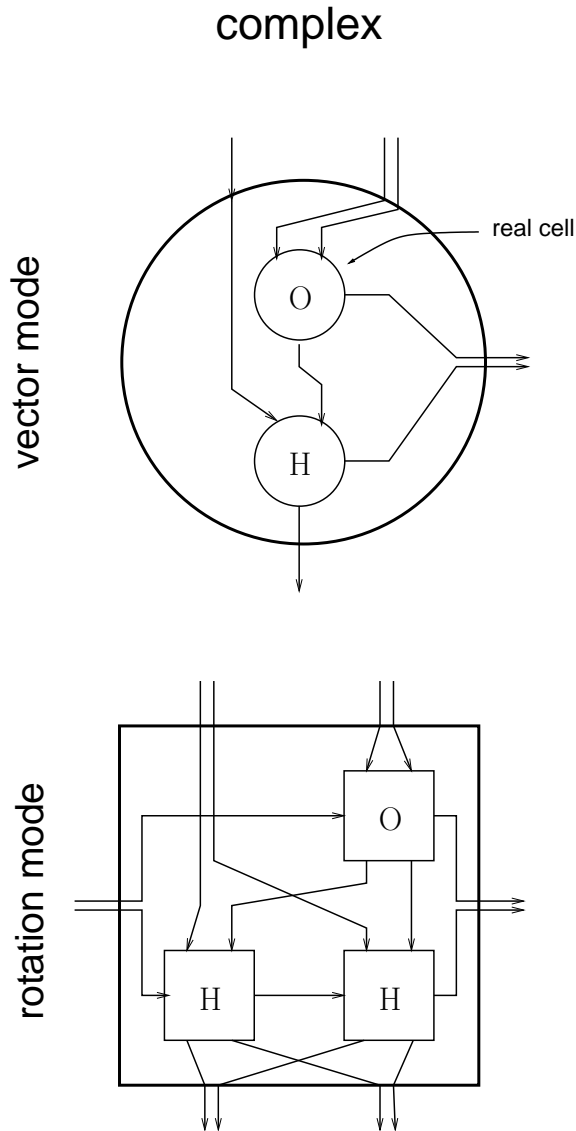
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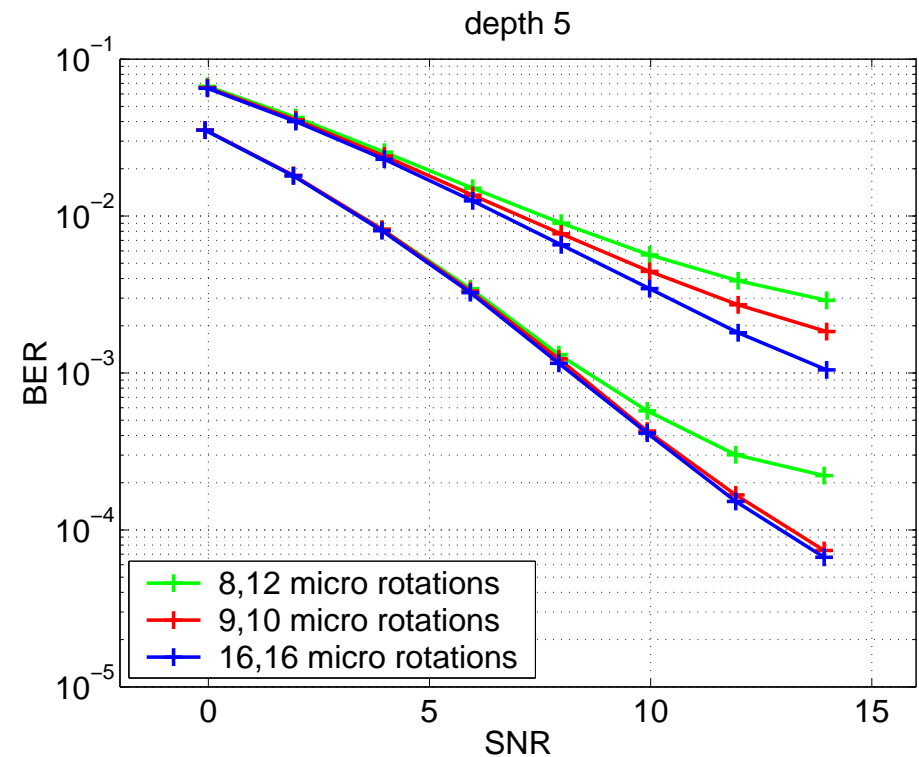
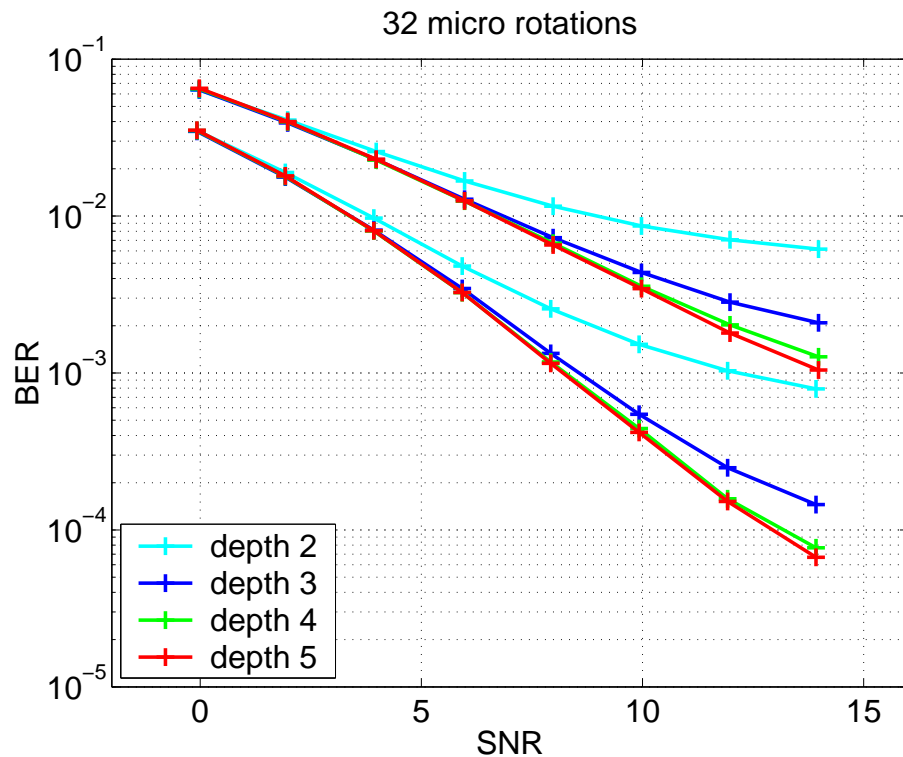


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Spreading factor 8, 6 active codes. 244 symbols/burst. Channel “Case 3”: 4 taps, 120 km/h, 57 chips, perfect channel estimation. CORDIC with IEEE double floats.

- 122 Schur steps for exact solution, 5 suffice.
 - 9 orthogonal, 10 hyperbolic micro rotations as good as double floats.
- (when looking at bit errors)

DSP: Cholesky algorithm, sequential.

exact: 3450000 real multiplications per burst.
1 burst per 10ms frame: 345 MFLOPS.

approximated: 479000 real multiplications / 48 MFLOPS.

ASIC: Schur algorithm, parallel.

exact: 5205 real CORDIC cells,
796 activations per cell.

approximated: $5205 \cdot 10 \cdot 2$ adder + $5205 \cdot 2$ constant multipliers,
94 activations per cell.

additionally: 505056 real multiplications for back substitution, either sequentially (50 MFLOPS) or parallel.