PRO-DASP

Power Reduction on Digital Audio Signal Processing

"PRO-DASP: Verlustleistungsabschätzung auf hoher Abstraktionsebene – Kommunikationsanteile und Ablaufplanung für Power-Management "

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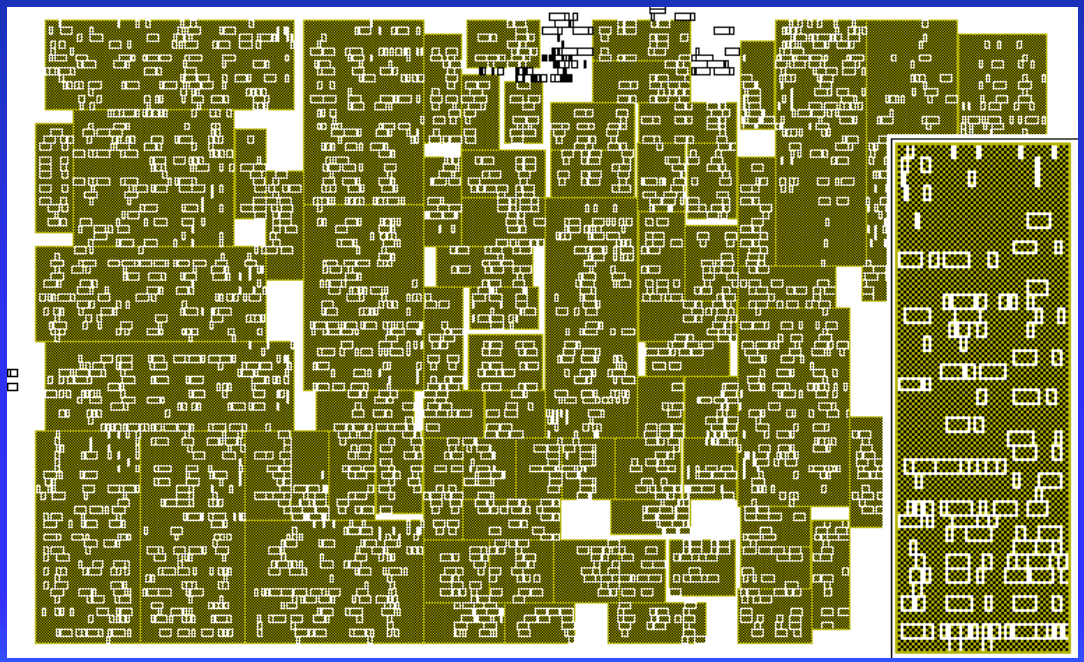
Outline

- Interconnect-power estimation: results
- Scheduling for power optimization
- Conclusion

Evaluation of Interconnect Power Estimation

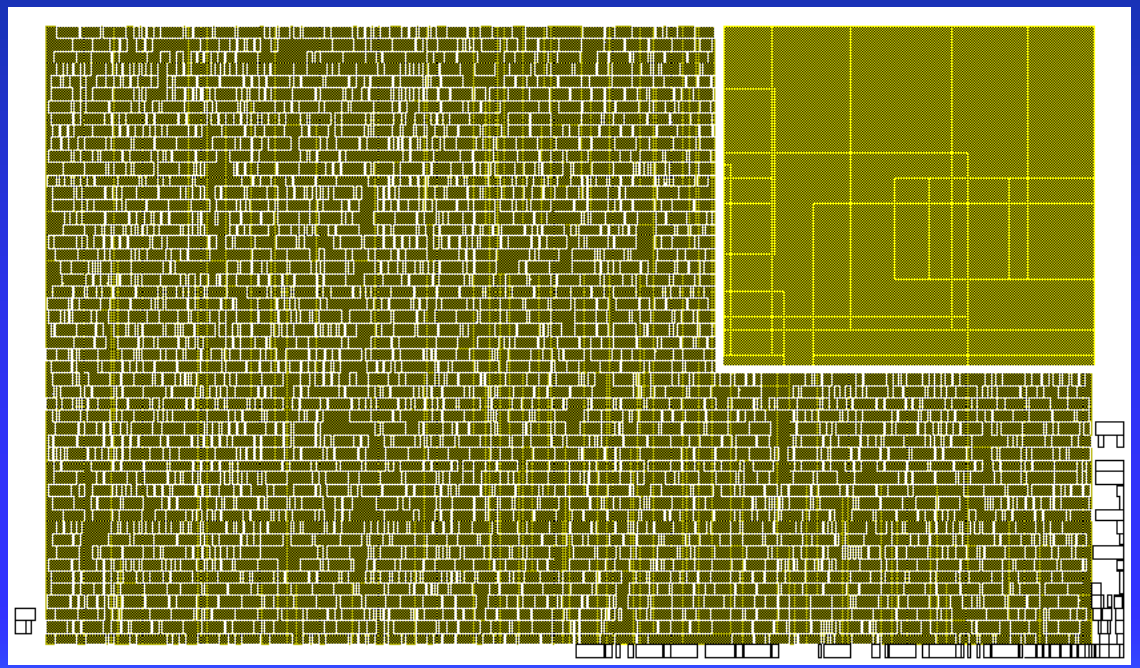
- Floorplan as described during Koll. 2002 in Chemnitz (improved Steiner-Tree)
- A floorplan is imposed to Silicon Ensemble by defining regions for RT-resources (dark rectangles).
- We choose region coordinates in the manner that Silicon Ensemble can place cells directly at the border of a region (enlarged section).



Forced floorplan of Silicon Ensamble (FDCT)

Evaluation (cont.)

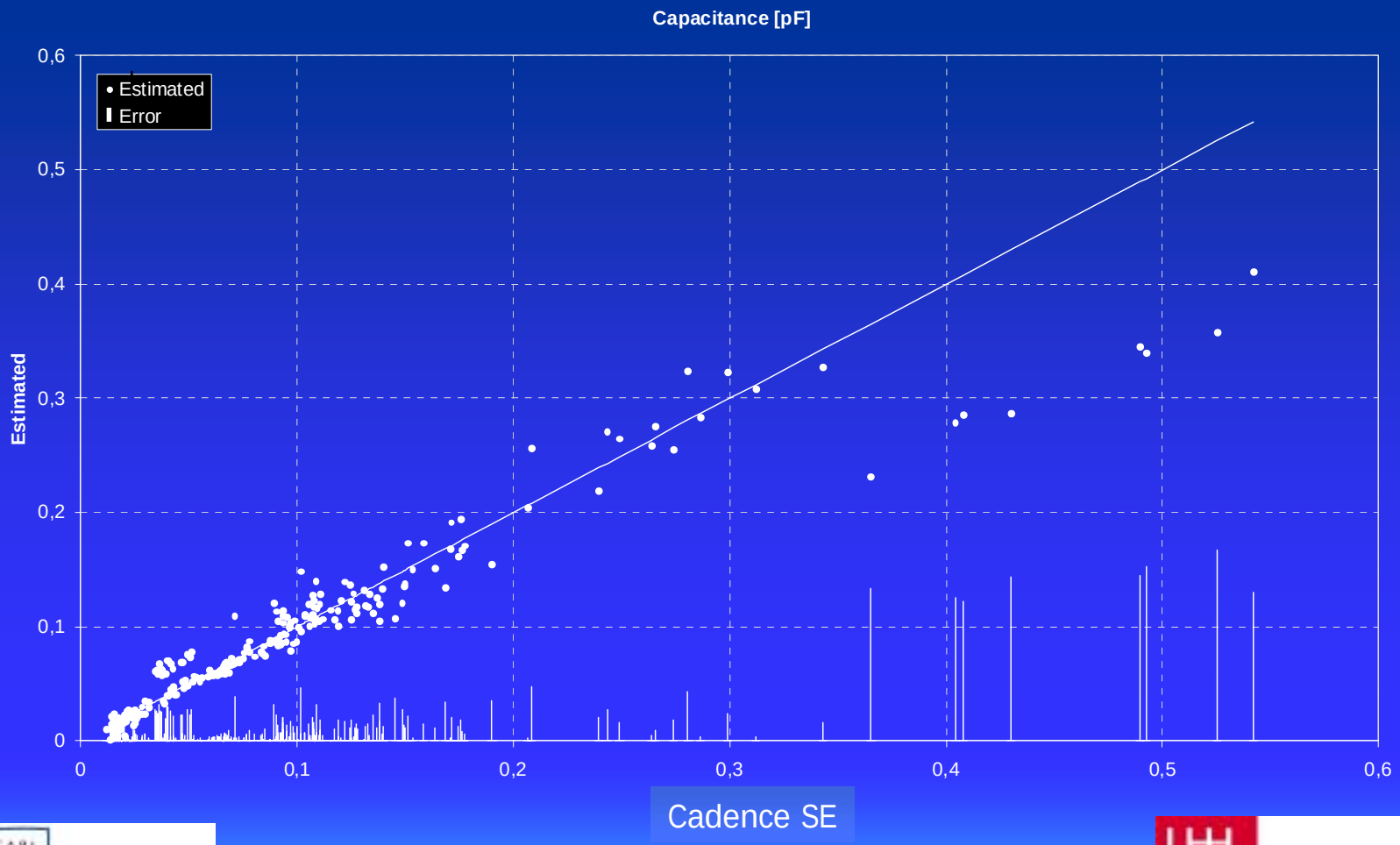
- The area of the regions is overestimated.
  - If only one cell could not be placed within a region Silicon Ensemble discontinue.
- To increase the utilization we overlap the regions sparsely (enlarged section).



Forced floorplan with overlapping (FDCT)

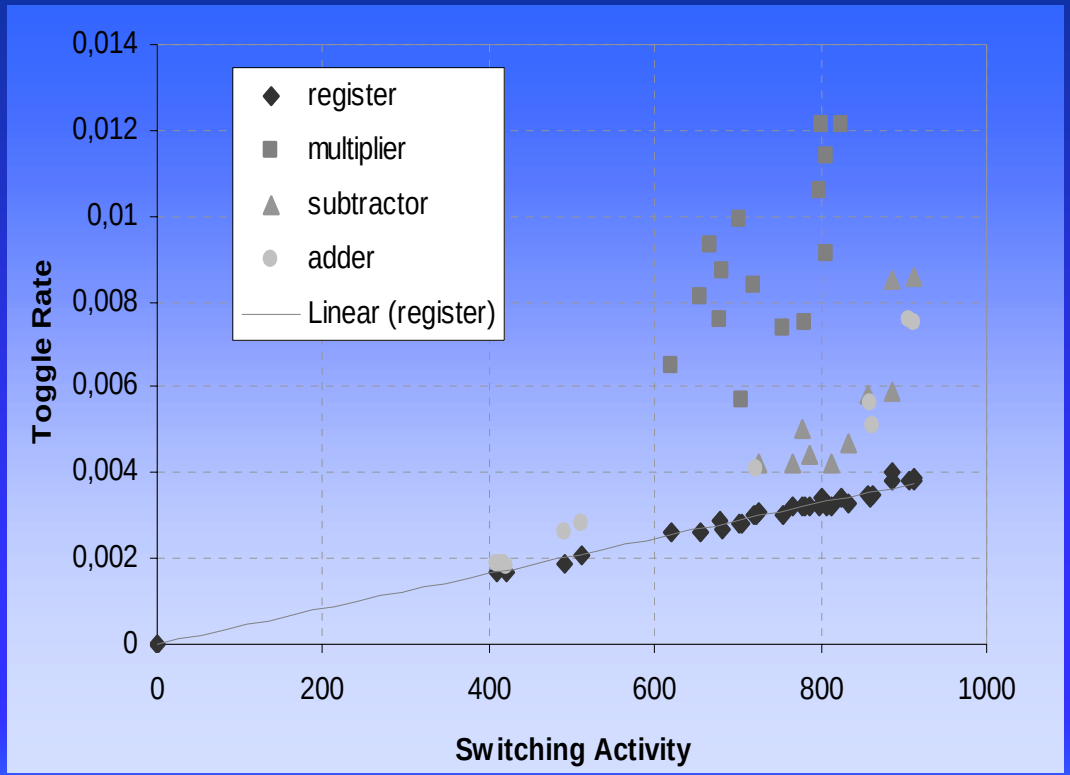
Capacitance Estimation

Estimated capacitance vs. Silicon Ensamble for a forced floorplan (FFT)



Activity Estimation

- We underestimate the activity by a factor of three for wires at the output of multiplier.
- We will focus our research effort in AVSy on a power model which covers this aspect (”spurios transitions“).



Effect of glitches on wire activity (FDCT)

New Scheduler

- Scheduler developed in EU-project uses simple ALAP scheduling
  - Main disadvantage: poor usage of resources
- New Scheduler uses „Force Directed Scheduling“ (FDS)
  - Medium complexity, with good results
  - Can handle large designs
  - Provides capabilities for delay calculation for different V_{dd}
  - Offers better solutions with regards to resource usage
- The scheduler...
  - first determines „movability“ by an ASAP+ALAP schedule,
  - calculates cost of each operation in every possible c-step
  - determines operation with minimum cost, which is scheduled
  - iterates until all operations are scheduled
- Enhanced capabilities:
  - resource contrained
  - memory pre-scheduling

New Scheduler

	9 csteps			14 csteps			50 csteps		
Scheduler	#ADD	#SUB	#MULT	#ADD	#SUB	#MULT	#ADD	#SUB	#MULT
FDS	1	1	2	1	1	1	1	1	1
ALAP	1	1	3	1	1	3	1	1	3

Resource count compared for old and new scheduling algorithm

Scheduler	#ADD	#SUB	#MULT
FDS	2	2	1
ALAP	4	2	1

Resource usage for a viterbi decoder, solutions of old and new scheduler

Scheduler	#ADD	#SUB	#MULT	Path length	Runtime
BC	1	1	2	9 csteps	32,12 sek
FDS	1	1	2	9 csteps	0,08 sek

Runtime of BC and FDS compared in time constraint mode

Conclusion

- Evaluation of interconnect Power Estimation
  - small errors for small capacitance
  - ”Spurious Transitions“ (→ AVSy)

- Resource-constrained FDS-Scheduler
  - memory pre-scheduling